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W800 Chip Design Guide

V1.8

Winner Micro

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1 Overview

The W800 chip is a secure IoT Wi-Fi/Bluetooth dual-mode SoC chip. Support 2.4G IEEE802.11b/g/n Wi-Fi communication protocol;

Support BT/BLE dual-mode working mode, support BT/BLE4.2 protocol. The chip integrates 32-bit CPU processor, built-in QFlash, SPI,

UART, GPIO, I2C, I2S, 7816 and other rich digital interfaces; support a variety of hardware encryption and decryption algorithms, built-in DSP, floating point unit

And security engine, support code security permission setting, built-in 2MBFlash memory, support firmware encrypted storage, firmware signature, security debugging,

A number of security measures such as security upgrades ensure product security features. Suitable for smart home appliances, smart homes, smart toys, wireless audio and video,

Wide range of IoT fields such as industrial control and medical monitoring.

2 Pin definition

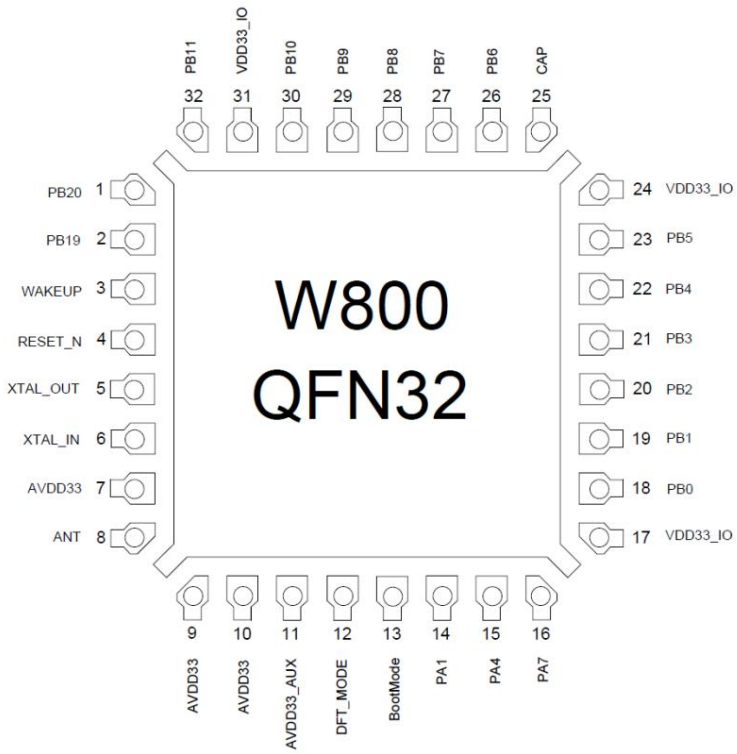


Figure 2-1 Pin layout diagram (QFN32)

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Table 2-1 Pin assignment definition (QFN32)

No.	Name	Type	Pin Function After Reset	multiplexing function	Highest frequency	pull-up and pull-down capability	drive capability
1	PB_20	I/O	UART_RX	UART0_RX/PWM1/UART1_CTS/I²C_SCL	10MHz	UP/DOWN	12mA
2	PB_19	I/O	UART_TX	UART0_TX/PWM0/UART1_RTS/I²C_SDA	10MHz	UP/DOWN	12mA
3	WAKEUP	I	WAKEUP wake up function			DOWN	
4	RESET	I	RESET Reset			UP	
5	XTAL_OUT	O	External crystal oscillator output				
6	XTAL_IN	I	External crystal oscillator input				
7	AVDD33	P	chip power supply, 3.3V				
8	ON	I/O	RF Antenna				
9	AVDD33	P	chip power supply, 3.3V				
10	AVDD33	P	chip power supply, 3.3V				
11	AVDD33_AUX	P	chip power supply, 3.3V				
12	TEST	I	Test function configuration pin				
13	BOOTMODE	I/O	BOOTMODE	I²S_MCLK/LSPI_CS/PWM2/I²S_DO	20MHz	UP/DOWN	12mA
14	PA_1	I/O	JTAG_CK	JTAG_CK/I²C_SCL/PWM3/I²S_LRCK/ADC0	20MHz	UP/DOWN	12mA

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15	PA_4	I/O	JTAG_SWO	JTAG_SWO/I²C_SDA/PWM4/I²S_BCK/ADC1	20MHz	UP/DOWN 12mA
16	PA_7	I/O	GPIO, input, high impedance	PWM4/LSPI_MOSI/I²S_MCK/I²S_DI/Touch0	20MHz	UP/DOWN 12mA
17	VDD33IO	P	IO power supply, 3.3V			
18	PB_0	I/O	GPIO, input, high impedance	PWM0/LSPI_MISO/UART3_TX/PSRAM_CK/Touch3	80MHz	UP/DOWN 12mA
19	PB_1	I/O	GPIO, input, high impedance	PWM1/LSPI_CK/UART3_RX/PSRAM_CS/Touch4	80MHz	UP/DOWN 12mA
20	PB_2	I/O	GPIO, input, high impedance	PWM2/LSPI_CK/UART2_TX/PSRAM_D0/Touch5	80MHz	UP/DOWN 12mA
21	PB_3	I/O	GPIO, input, high impedance	PWM3/LSPI_MISO/UART2_RX/PSRAM_D1/Touch6	80MHz	UP/DOWN 12mA
22	PB_4	I/O	GPIO, input, high impedance	LSPI_CS/UART2_RTS/UART4_TX/PSRAM_D2/Touch7	80MHz	UP/DOWN 12mA
23	PB_5	I/O	GPIO, input, high impedance	LSPI_MOSI/UART2_CTS/UART4_RX/PSRAM_D3/Touch8	80MHz	UP/DOWN 12mA
24	VDD33IO	P	IO power supply, 3.3V			
25	CAP	I	External capacitor, 4.7μF			
26	PB_6	I/O	GPIO, input, high impedance	UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK/Touch9	50MHz	UP/DOWN 12mA

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27	PB_7	I/O GPIO, input, high impedance		UART1_RX/MMC_CMD/HSPI_INT/SDIO _CMD/Touch10	50MHz	UP/DOWN 12mA	
28	PB_8	I/O GPIO, input, high impedance		I² S_BCK/MMC_D0/PWM_BREAK/SDIO_D 0/ Touch11	50MHz	UP/DOWN 12mA	
29	PB_9	I/O GPIO, input, high impedance		I² S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/ Touch12	50MHz	UP/DOWN 12mA	
30	PB_10	I/O GPIO, input, high resistance		I²S_DI/MMC_D2/HSPI_DI/SDIO_D2	50MHz	UP/DOWN 12mA	
31	VDD33IO	P	IO power supply, 3.3V				
32	PB_11	I/O GPIO, input, high impedance		I²S_DO/MMC_D3/HSPI_DO/SDIO_D3	50MHz	UP/DOWN 12mA	
33	GND	P ground					

Note: 1. I = Input, O = Output, P = Power

3 Chip Peripheral Circuit Design

3.1 RESET reset circuit design

The reset circuit is recommended to be designed as an RC circuit, which automatically resets when power-on, and W800 low-level reset. If using an external control RESET tube pin, when the level value is lower than 2.0v, the chip is in reset state. The low level must last for more than 100us when reset, see Figure 3-1.

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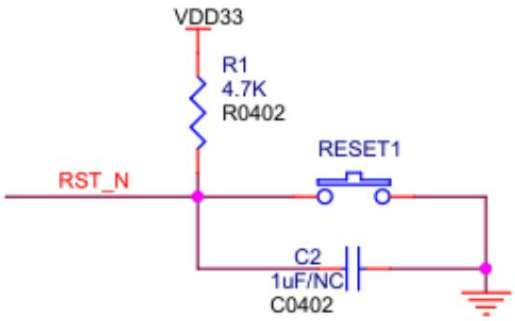


Figure 3-1 Reset circuit

3.2 Reference Clock Circuit Design

The chip reference clock uses 40MHz frequency, and customers choose different temperature grades, stability, and load capacitance values according to actual product requirements.

of crystals. The load capacitance connected to both ends of the crystal needs to be adjusted according to the crystal Cload value and frequency deviation of different manufacturers. See Figure 3-

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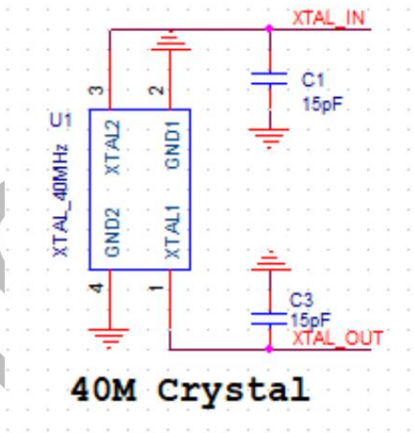


Figure 3-2 Crystal circuit

The crystal should be placed as close to the chip as possible, the wiring should be as short as possible, and far away from interference sources, and the crystal should be isolated by multiple ground holes. Layers below the clock prohibit its

It is routed through to prevent interfering with the clock source. There is no need for hollowing out under the crystal oscillator.

3.3 ADC circuit design

The 14-pin (PA1) and 15-pin (PA4) of the chip can be used as an ordinary ADC, and the input voltage range is 10mV~2.3V. when higher than

At 2.3V, the external part needs to be divided before entering the ADC interface. When using the voltage divider method, in order to improve the accuracy, R1 and R2 need to use high-precision

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resistance. Select the appropriate R1 and R2 resistance value to divide the voltage according to the Sensor output voltage value. As shown in Figure 3-3.

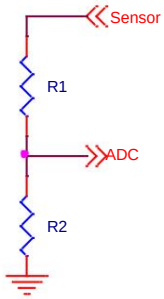


Figure 3-3 ADC voltage divider circuit

3.4 RF circuit design

The chip adopts a single-antenna design, and integrates a power amplifier and a transceiver switch inside. The impedance of the chip's RF port is 17-1.5jÿ. According to the actual product design

According to the performance matching requirements of the meter, it is necessary to reserve the reference design matching network in Figure 3-8, and optimize the external design matching components according to the actual antenna impedance value.

The components need to be designed in the form of low-pass, and the ability to suppress the second harmonic is more than 10dB.

3.5 GPIO Design

After the chip is powered on, pins 1 and 2 default to UART0 ports, which provide download and AT command ports and log output ports. customer use

Be careful not to use this port as GPIO arbitrarily to prevent it from being occupied and unable to download and debug. After the system is up, the port can be reset

Used for other ports. If this port is occupied, you can operate according to Section 3.6.

Table 3-2 Chip UART0 pin description

1	PB20	I/O	UART0_RX
2	PB19	I/O	UART0_TX

The multiplexing relationship and use of other pins are shown in Table 2-1. If all GPIOs are equipped with pull-up resistors, the typical pull-up resistor value is 40K, if

Configured as pull-down, the typical pull-down resistor value is 49K.

The Wakeup pin is an external wake-up pin. When the chip enters the sleep state and the Wakeup pin is given a high level, the chip wakes up. normal working status

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state, the port is low.

The TEST pin is the chip test pin, which is floating.

3.6 Download port

The W800 chip defaults UART0 as the download port. When the chip has no firmware for initial download, it is directly connected to the UART0 interface and downloaded through the relevant download software.

to download the firmware. When there is firmware in the chip, enter the download mode again, you can enter the download mode by pulling down PA0, and then power on.

After the download is complete, remove the operation of pulling PA0 low, and restart the firmware to run.

3.7 Power Supply Design

Corresponding filter capacitors should be placed on the input pin of the chip power supply to improve product performance. It is recommended to use an LDO for external power supply to the entire chip, and the total current is recommended to be

500mA and above are recommended. The total power line width requirement is not less than 30mil. The power supply range is 3.0V-3.6V. Do not exceed this range, more than 3.6V

May cause permanent damage to the chip. Below 3.0V may cause system instability and overall performance degradation. See below for placement of capacitors on different pins

above requirements.

A 1uf filter capacitor needs to be placed on pin 7 of the chip.

A 1nf filter capacitor needs to be placed on pin 9 of the chip. See Table 3-3.

Table 3-3 Chip power pin description

7	VDD33	P	chip power supply, 3.3V	
9	VDD33LNA	P	LNA power supply, 3.3V	

A 47uf filter capacitor is placed near pin 10 of the chip.

A 47uf filter capacitor is placed near pin 11 of the chip.

It is recommended that customers place a 330uf electrolytic capacitor at the power inlet of the module. See Table 3-4.

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Table 3-4 Chip power pin description

10	VDD33PA	P	PA power supply, 3.3V	
11	VDD33AUX	P	Analog power supply, 3.3V	

1uf filter capacitors can be placed near pins 17, 24, and 31 of the chip according to conditions. See Table 3-5.

Table 3-5 Chip power pin description

17	VDD33IO	P	IO power supply, 3.3V	
24	VDD33IO	P	IO power supply, 3.3V	
31	VDD33IO	P	IO power supply, 3.3V	

The chip's 25-pin CAP must be connected with a 4.7uf filter capacitor.

3.8 Anti-static design

In order to improve the anti-static capability of the chip, it is necessary to place an anti-static ESD protection device on the antenna end. The antenna uses an inverted F antenna. The matching circuit is shown in the figure 3-8 shown. Do a good job of electrostatic protection during the production process. Please refer to the schematic diagram and BOM table for recommended models of anti-static devices. In order to meet the needs of production testing, the RF test point TP2 can be reserved on the back of the module.

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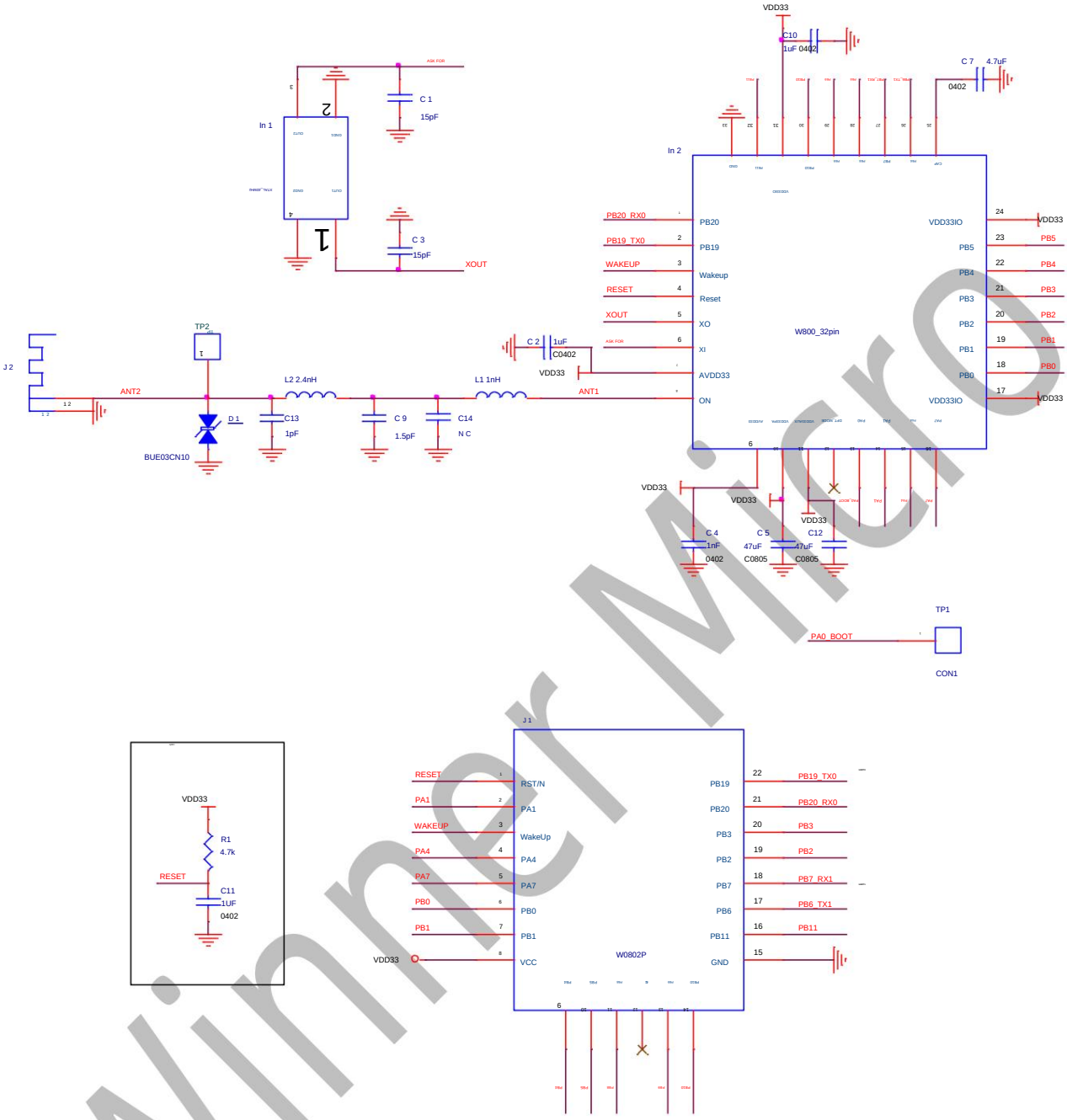


Figure 3-8 Schematic diagram and location of ESD tube

4 Layout design

The PAD in the middle of the W800 chip is a heat-dissipating pad, which needs to be grounded. At the same time, a ground hole needs to be drilled to make good contact with the ground for heat dissipation. The middle belly

Do not make window design for vias. As shown in Figure 4-1.

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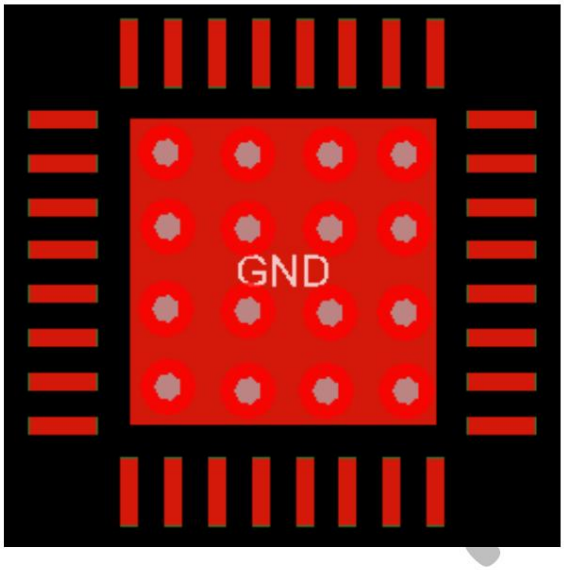


Figure 4-1 Ground pad treatment

After the product design is completed, all layers of the PCB need to be grounded with copper. It is necessary to ensure that the ground plane of the RF traces on the second layer is complete.

To ensure the continuity of RF impedance, and the RF trace needs to be controlled with 50 ohm impedance according to the thickness of the board.

Do not expose copper on the BOTTOM layer of the PCB.

It is recommended to use a star-shaped wiring for the power supply, see Figure 4-2 for the highlighted part of the wiring. Pay special attention to the 9-pin power supply pin do not directly connect with 10,11 pins

From the beginning, each power supply pin adopts a star-shaped wiring. Except for the digital IO power supply pin, each other power supply pin has a single power line to the main power supply to avoid

The internal power supplies crosstalk each other. All capacitors connected to chip power pins should be placed close to the chip power pins.

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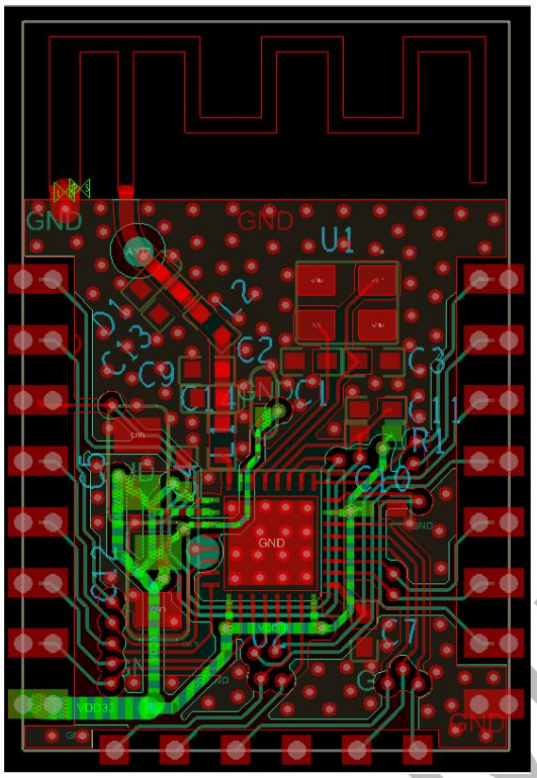


Figure 4-2 Power star wiring

5 Antenna Design

According to customer needs, an external antenna or a PCB onboard antenna can be used. Different antennas may have different effects on product performance

Influence, the matching components need to be adjusted according to the antenna impedance.

5.1 External Antenna

The connection socket for connecting the external antenna should be as far away as possible from noise sources such as power supply on the bottom board to prevent interference with the antenna.

5.2 Onboard Antenna

When the module is designed with a PCB onboard antenna, it must be designed in strict accordance with this guide to prevent the performance of the antenna from degrading and affecting the use of the product.

The copper on the back of the antenna needs to be completely hollowed out. The reference ground plane of the antenna should be as large as possible. The highlighted green area is the antenna part, and all layers in the green area are not covered.

Can be coated with copper, all clear. And the PCB in the green antenna area needs to be covered with oil, and the exposed copper skin of the antenna is prohibited. The yellow highlighted area is the RF matching

50 ohm impedance control is required for matching devices and routing areas. See Figure 5-1.

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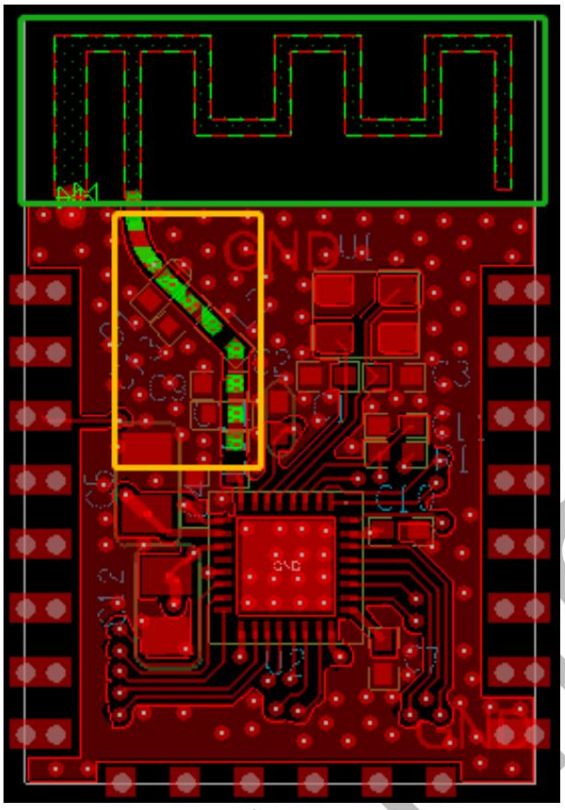


Figure 5-1 Suggested antenna layout

Figure 5-2 Antenna placement methods that are commonly used and have little impact on antenna performance. Try to ensure that there are no physical blocking objects around the antenna.

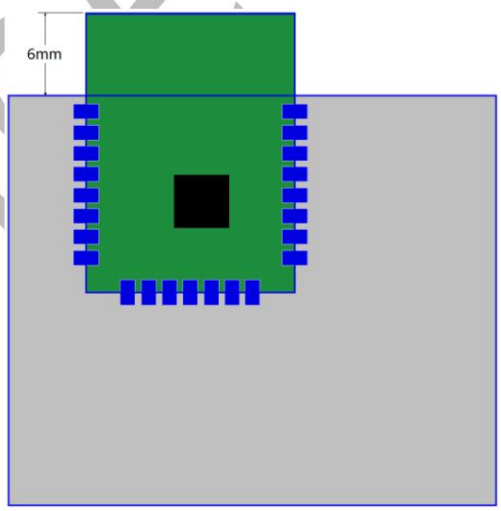


Figure 5-2

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